

I claim:

1. A method for transforming a logical hierarchy associated with a model of  
2 an electronic design into a physical hierarchy optimized for chip-level implementation of  
3 that electronic design, the method comprising:

4 partitioning the model into a number of data-flow-logic partitions and control  
5 logic partitions, each partition having a boundary; and  
6 selectively readjusting partition boundaries in response to placement based  
7 information thereby forming a physical hierarchy based on  
8 connectivity between partitions.

1. 2. A method for partitioning an electronic design into a number of data-flow-logic partitions, the method comprising:

3 traversing the electronic design to group data operators inter-connected by  
4 buses into data-flow-logic partitions, wherein data operators inter-  
5 connected by an independent bus system form an independent data-  
6 flow partition; and  
7 selectively breaking or merging each of the data-flow-logic partitions based on  
8 placement-based information.

*add a 27*